Regular Paper

Integral Formation of Circuit and Bump by Plating Process without Chemical Mechanical Polishing (CMP)

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Received Nov. 2, 2017; accepted for publication Nov. 15, 2017

Abstract

In order to form a bump on an existing circuit, after forming a plating resist having an open portion that would become a bump on the circuit, plating is performed with a thickness equal to or greater than the thickness of the resist to form a mushroom-shaped bump. These mushroom-shaped bumps are polished by CMP, whereby it is possible to form bumps having a uniform height and a flat top. However, this kind of process is complicated and advanced techniques are required. Furthermore, as circuits and bumps are become more miniaturized, it is also difficult to achieve the necessary adhesion strength between the circuit and the bumps as well as the circuit and the materials. By using the formation method that we examined, we were able to form circuit-integrated bumps of uniform height and flat top without using CMP.

Keywords: Bump, Electroplating, Photolithography

1. Introduction

With the expansion of telecommunications including IoT (Internet of Things), electronic devices such as smartphones and tablets have made remarkable progress. The development of such electronic devices is supported by fine circuit processing technologies using plating, which contributes to miniaturization and high functionality.

Bumps are provided as electrodes for flip-chip mounting which can accommodate high density packaging. Generally, bumps are formed by a plating method using a photoresist pattern; however, this method has the following problems.

In order to achieve high-density packaging, it is necessary to narrow the pitch of the plating resist opening that becomes a bump due to narrowing of the pitch between the bumps. When bump formation is performed by electroplating, the current concentrates on the outer peripheral portion due to the effect of the primary current distribution and the film thickness of the outer peripheral portion tends to become thick. For this reason, it is difficult to obtain uniform bump height over the entire surface. As a countermeasure to this, shielding plates are placed between the anode and the substrate, or an auxiliary anode is used to make the current distribution uniform. However, it is difficult to optimize due to constraints of plating equipment and plating conditions. For this reason, plating is performed to a thickness greater than the resist pattern thickness to form a mushroom-like bump. Thereafter, uniformity of the bump height and flatness of the top of the bumps are ensured by CMP. However, advanced flat polishing techniques are required. In addition, there are concerns about defects such as voids in the bumps and adhesion between bumps and the circuit. There is an apprehension that voids would lead to an increase in electrical resistance and deterioration of electro-migration resistance[1], and hence it lacks connection reliability as well as insulation reliability. Furthermore, the finer the bumps are, the smaller the adhesive area with the circuit becomes, making it difficult to secure adhesion between the bumps and the circuit.

Given that, in this study, we examined a method of forming

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