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Shape Control of Floating Si Wires Fabricated by Anodization

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Abstract

We fabricated silicon wires of different thicknesses, shapes, and crystal types on wafers with pre-etched dislocations using anodization with a hydrogen fluoride and ethanol mixture. Control of the groove outlines for dislocation made various wire configurations possible. The crystallinity of the wires was controlled by crystal face selection. The wires featured a porous surface and crystalline ends when formed on a (100) Si wafer crystal face. On the other hand, entirely porous Si wires were formed when using wafers with a (111) crystal face. In addition, the capacity of these wires for future device use was examined based on the wire crystallinity. Moreover, we discussed the formation mechanism of these wires based on their shapes, where carrier transport in the wafer during anodization played a key role.

Keywords: Si wire, shape control, dislocation, anodization, porous Si

1. Introduction

Micronanostructured silicon wires are anticipated as important components in future devices such as waveguides and modulators for optical communication devices [1–3] and photonic integrated circuits (ICs) [4–6]. These wires are typically fabricated using traditional lithography techniques, where the wires are formed on silicon wafers. As a result, they are directly connected to the wafer surface, restricting the possible wire shapes that can be formed. The contact area between the wires and the surface of the wafer can lead to carrier leakage, electro-magnetic effects, carrier transport and indexing issues for photo integrated circuits. Furthermore, this contact reduces the freedom of the wiring. Previously, we developed a new method for fabricating Si wires using anodization after introducing dislocations into crystalline Si [7]. Wires made in this manner have hybrid structures (with porous surfaces and crystalline bottom layers) and freestanding structures. In addition, our free-standing floating Si wire has free space around the wire. Such wires are expected to boost device performance, and new use cases are possible that utilize the space around the wires. Control of the wire shape and crystallinity is needed for such systems in order to develop new devices using floating wires. However, control of the wire size and crystallinity (crystalline or porous) is not well established for these systems, as introducing the dislocations in a controlled manner is difficult. Furthermore, connections and curves are required of these wires to achieve high performance and multi-functional devices. This paper reports the fabrication of wires having various controlled configurations (such as lines, curves and crosses) using anodization after introducing dislocations. The formation mechanism of these dislocations is also discussed.

2. Experimental methods

P-type (100) and (111) crystalline silicon wafers formed by the Czochralski process were used as starting materials. The resistivity and thickness of the wafers ranged from 1–100 Ω·cm and 0.525–0.625 mm, respectively. The wires were fabricated by anodization after forming grooves on the silicon wafer surfaces using metal or diamond tip pens. The head radius of the metal pen (GENERAL, Tungsten carbide point scriber/etching pen, # 88) was 70 μm, while the radius of the diamond one (Tokyo seimitsu, Stylus of surface texture and contour measuring

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